



**4G bits DDR3(L) SDRAM DATA SHEET**  
**(1024M words x 4 bits)**  
**(512M words x 8 bits)**  
**(256M words x 16 bits)**

**Revision 0.2**

**Aug. 2019**

## Revision History

Revision No.	History	Draft date	Remark
0.0	Initial Draft	Mar.20.2019	preliminary
0.1	Modify catalog, page num, and add ordering information etc	May.14.2019	
0.2	Modify document title for A version only	Aug.15.2019	

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## Specifications

- Density: 4G bits
- Organization
  - 128M word x4 bits x 8 banks
  - 64M word x8 bits x 8 banks
  - 32M word x16 bits x 8 banks
- Package
  - 78-ball FBGA(X4/X8)
  - 96-ball FBGA(X16)
  - Lead-free (RoHS compliant) and Halogen-free
- Power supply: 1.35V (typ) of 1600
  - VDD = 1.283V to 1.45V
  - Backward compatible for VDD, VDDQ = 1.5V ± 0.075V
- Power supply: 1.5V ± 0.075V (typ) of 1866
- Data rate
  - 1600Mbps/1333 Mbps (1.35V)
  - 1866 Mbps (1.5V)
- 1KB page size
  - Row address: A0 to A15(X4/X8)
  - Column address: A0 to A9,A11(X4)
- 2KB page size A0 to A9(X8)
  - Row address: A0 to A14(X16)
  - Column address: A0 to A9(X16)
- Eight internal banks for concurrent operation
- Burst length (BL): 8 and 4 with Burst Chop (BC)
- Burst type (BT):
  - Sequential (8, 4 with BC)
  - Interleave (8, 4 with BC)
- /CAS Latency (CL): 5, 6, 7, 8, 9, 10, 11,13(1866)
- /CAS Latency (CL): 5, 6, 7, 8, 9, 10, 11(1600/1333)
- /CAS Write Latency (CWL): 5, 6, 7, 8,9(1866)
- /CAS Write Latency (CWL): 5, 6, 7, 8(1600/1333)
- Precharge: auto precharge option for each burst access
- Driver strength: RZQ/7, RZQ/6 (RZQ = 240Ω)
- Refresh: auto-refresh, self-refresh
- Refresh cycles
  - Average refresh period
  - 7.8μs at 0°C ≤ TC ≤+85°C
  - 3.9μs at +85°C < TC ≤+95°C
- Operating case temperature range
  - TC = 0°C to +95°C

## Features

- Double-data-rate architecture: two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted /CAS by programmable additive latency for better command and data bus efficiency
- On-Die Termination (ODT) for better signal quality
  - Synchronous ODT
  - Dynamic ODT
  - Asynchronous ODT
- Multi Purpose Register (MPR) for pre-defined pattern read out
- ZQ calibration for DQ drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- /RESET pin for Power-up sequence and reset function
- SRT range:
  - Normal/extended
- Programmable Output driver impedance control

# Part Number

**FM 3 XX XX X A X – X X X X**

**Dosilicon  
Memory**

**Product Family**  
3: Consumer DDR3 SDRAM

**Device Depth**  
8E: 2G/8K ref  
8F: 4G/8K ref

**Organization**  
08 : x8  
16 : x16

**Interface**  
S : STTL

**Generation**  
A : 1<sup>st</sup>  
B : 2<sup>nd</sup>

**Package Type**  
A : 78ball FBGA, 7.5 x 11mm<sup>2</sup>, 1.2T max  
B : 96ball FBGA, 7.5 x 13.5mm<sup>2</sup>, 1.2T max  
C : 78ball FBGA, 9x10.5mm<sup>2</sup>, 1.2T max  
D : 96ball FBGA, 9x13.5mm<sup>2</sup>, 1.2T max

**Temperature**  
B: -40°C ~ 95°C  
D: 0°C ~ 95°C

**Power Supply**  
F: VDD/VDDQ = 1.5V  
G: VDD/VDDQ = 1.35V

**CL-tRCD-tRP**  
H : 9-9-9  
K : 11-11-11  
M : 13-13-13

**Clock Frequency(Data Rate)**  
6 : 667MHz(1333Mbps)  
8 : 800MHz(1600Mbps)  
9 : 933MHz(1866Mbps)

## Ordering Information

Part Number	Density	Voltage	Speed	Temp. Range	PKG Type
FM38F16SAD-8KGD	4Gb	1.35V/1.5V	800MHz	0°C~95°C	FBGA 96(9*13.5*1.2mm)
FM38F16SAD-9MFD		1.5V	933MHz		FBGA 96(9*13.5*1.2mm)

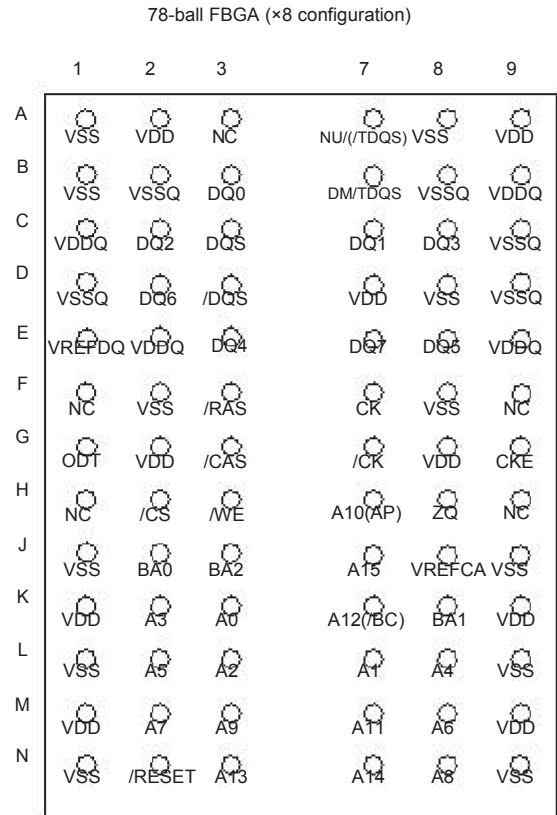
Pin Configurations

Pin Configurations (\*4/\*8 configuration)

/xxx indicates active low signal.



(Top view)



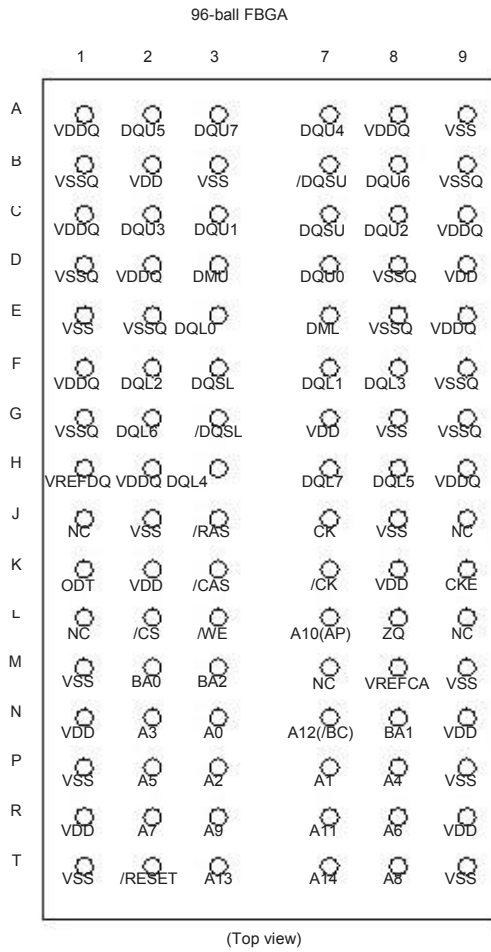
(Top view)

Pin name	Function	Pin name	Function
A0 to A15 <sup>3</sup>	Address inputs A10(AP): Auto precharge A12(/BC): Burst chop	RESET <sup>3</sup>	Active low asynchronous reset
BA0 to BA2 <sup>*</sup>	Bank select	VDD	Supply voltage for internal circuit
DQ0 to DQ7	Data input/output	VSS	Ground for internal circuit
DQS, /DQS	Differential data strobe	VDDQ	Supply voltage for DQ circuit
TDQS, /TDQS	Termination data strobe	VSSQ	Ground for DQ circuit
/CS <sup>3</sup>	Chip select	VREFDQ	Reference voltage for DQ
/RAS, /CAS, /WE <sup>*</sup>	Command input	VREFCA	Reference voltage for CA
CKE <sup>*</sup>	Clock enable	ZQ	Reference pin for ZQ calibration
CK, /CK	Differential clock input	NC <sup>1</sup>	No connection
DM	Write data mask	NU <sup>2</sup>	Not usable
ODT <sup>*</sup>	ODT control		

- Notes:
1. Not internally connected with die.
  2. Don't connect. Internally connected.
  3. Input only pins (address, command, CKE, ODT and /RESET) do not supply termination.

**Pin Configurations (× 16 configuration)**

/xxx indicates active low signal.



Pin name	Function	Pin name	Function
A0 to A14 <sup>2</sup>	Address inputs A10(AP): Auto precharge A12(BC): Burst chop	/RESET <sup>2</sup>	Active low asynchronous reset
BA0 to BA2 <sup>2</sup>	Bank select	VDD	Supply voltage for internal circuit
DQU0 to DQU7 DQL0 to DQL7	Data input/output	VSS	Ground for internal circuit
DQSU, /DQSU DQSL, /DQSL	Differential data strobe	VDDQ	Supply voltage for DQ circuit
/CS <sup>2</sup>	Chip select	VSSQ	Ground for DQ circuit
/RAS, /CAS, /WE <sup>2</sup>	Command input	VREFDQ	Reference voltage for DQ
CKE <sup>2</sup>	Clock enable	VREFCA	Reference voltage for CA
CK, /CK	Differential clock input	ZQ	Reference pin for ZQ calibration
DMU, DML	Write data mask	NC <sup>1</sup>	No connection
ODT <sup>2</sup>	ODT control		

Notes: 1. Not internally connected with die.  
2. Input only pins (address, command, CKE, ODT and /RESET) do not supply termination.

## 1. Electrical Conditions

- All voltages are referenced to VSS (GND)
- Execute power-up and Initialization sequence before proper device operation is achieved.

### 1.1 Absolute Maximum Ratings

Table 1: Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Power supply voltage	VDD	- 0.4 to +1.975	V	1, 3
Power supply voltage for output	VDDQ	- 0.4 to +1.975	V	1, 3
Input voltage	VIN	- 0.4 to +1.975	V	1
Output voltage	VOUT	- 0.4 to +1.975	V	1
Reference voltage	VREFCA	- 0.4 to $x 0.6 \times VDD$	V	3
Reference voltage for DQ	VREFDQ	- 0.4 to $x 0.6 \times VDDQ$	V	3
Storage temperature	Tstg	-55 to +100	°C	1, 2
Power dissipation	PD	1.0	W	1
Short circuit output current	IOUT	50	mA	1

- Notes:
1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
  2. Storage temperature is the case surface temperature on the center/top side of the DRAM.
  3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must be no greater than  $0.6 \times VDDQ$ . When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

Caution: Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### 1.2 Operating Temperature Condition

Table 2: Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Notes
Operating case temperature	TC	0 to +95	°C	1, 2, 3

- Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM.
  2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C to +85°C under all operating conditions.
  3. Some applications require operation of the DRAM in the Extended Temperature Range between +85°C and +95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
    - a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9µs. (This double refresh requirement may not apply for some devices.)
    - b) If Self-refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 bit [A6, A7] = [0, 1]) or enable the optional Auto Self-Refresh mode (MR2 bit [A6, A7] = [1, 0]).

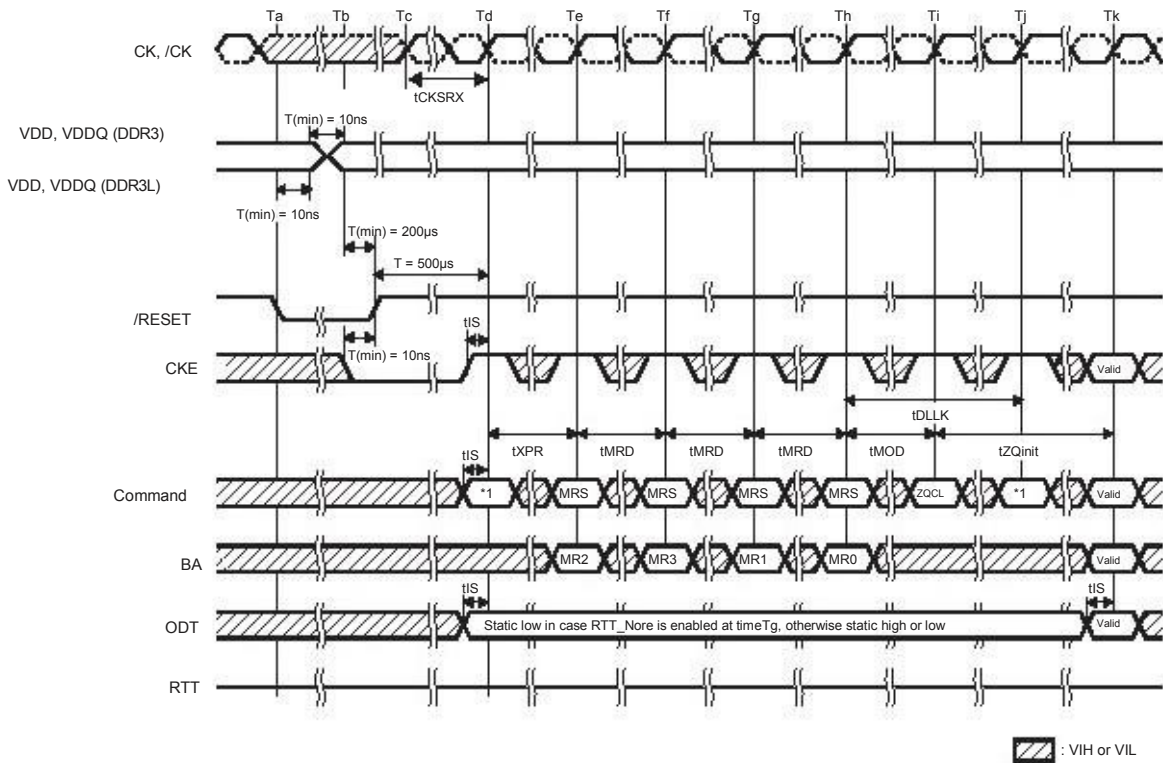


1.3 Recommended DC Operating Conditions

Table 3: Recommended DC Operating Conditions (TC = 0°C to +85°C), DDR3L Operation

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply voltage	VDD	1.283	1.35	1.45	V	1, 2, 3, 4
Supply voltage for DQ	VDDQ	1.283	1.35	1.45	V	1, 2, 3, 4

- Notes :
1. Maximum DC value may not be greater than 1.425V. The DC value is the linear average of VDD/VDDQ(t) over a very long period of time (e.g. 1 sec).
  2. If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
  3. Under these supply voltages, the device operates to this DDR3L specification.
  4. Once initialized for DDR3L operation, DDR3 operation may only be used if the device is in reset while
  5. VDD and VDDQ are changed for DDR3 operation shown as following timing wave form.



Note: 1. From time point Td until Tk, NOP or DES commands must be applied between MRS and ZQCL commands.

Figure 1: VDD/VDDQ Voltage Switch between DDR3L and DDR3

## 1.4 IDD and IDDQ Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined.

The figure Measurement Setup and Test Load for IDD and IDDQ Measurements shows the setup and test load for IDD and IDDQ measurements.

- IDD currents (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET, IDD6TC and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.

Note:IDDQ values cannot be directly used to calculate I/O power of the DDR3 SDRAM. They can be used to support correlation of simulated I/O power to actual I/O power as outlined in correlation from simulated channel I/O power to actual channel I/O power supported by IDDQ measurement.

For IDD and IDDQ measurements, the following definitions apply:

- L and 0:  $V_{IN} \leq V_{IL(AC)max}$
- H and 1:  $V_{IN} \geq V_{IH(AC)min}$
- MID-LEVEL: defined as inputs are  $V_{REF} = V_{DDQ} / 2$
- FLOATING: don't care or floating around  $V_{REF}$ .
- Timings used for IDD and IDDQ measurement-loop patterns are provided in Timings used for IDD and IDDQ Measurement-Loop Patterns table.
- Basic IDD and IDDQ measurement conditions are described in Basic IDD and IDDQ Measurement Conditions table.

Note:The IDD and IDDQ measurement-loop patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.

- Detailed IDD and IDDQ measurement-loop patterns are described in IDD0 Measurement-Loop Pattern table through IDD7 Measurement-Loop Pattern table.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting.
  - RON = RZQ/7 (34Ω in MR1);
  - Qoff = 0B (Output Buffer enabled in MR1);
  - RTT\_Nom = RZQ/6 (40Ω in MR1);
  - RTT\_WR = RZQ/2 (120Ω in MR2);
  - TDQS Feature disabled in MR1
- Define D = {/CS, /RAS, /CAS, /WE} : = {H, L, L, L}
- Define /D = {/CS, /RAS, /CAS, /WE} : = {H, H, H, H}

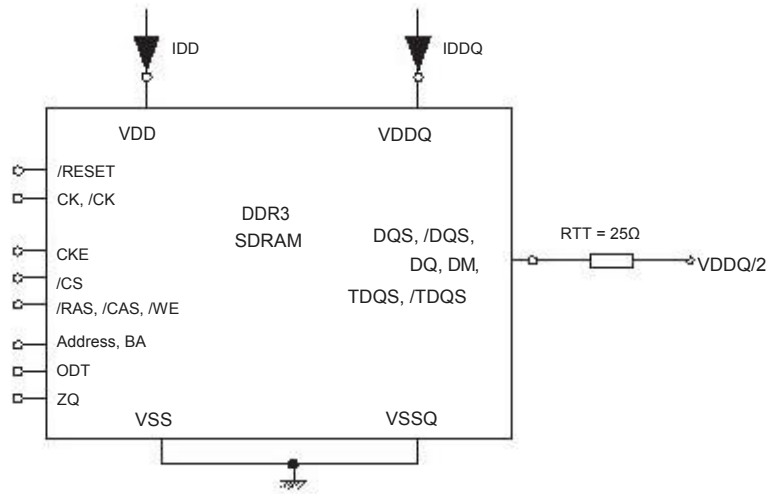


Figure 2: Measurement Setup and Test Load for IDD and IDDQ Measurements

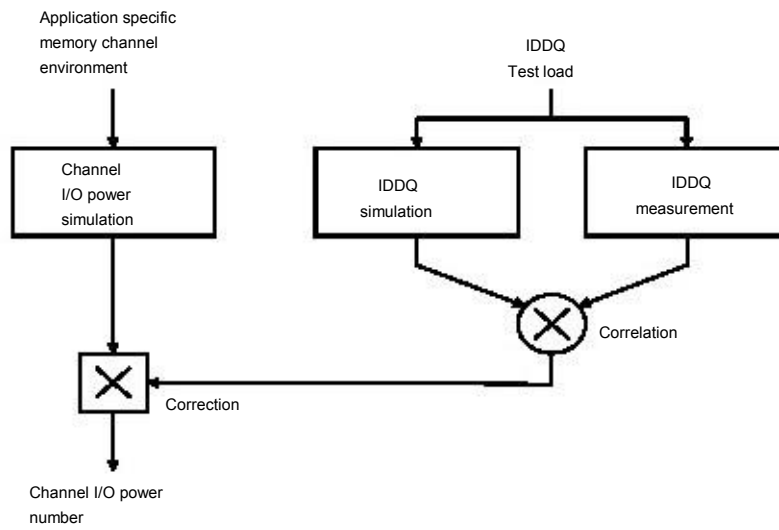


Figure 3: Correlation from Simulated Channel I/O Power to Actual Channel I/O Power Supported by IDDQ Measurement

## 1.4.1 Timings Used for IDD and IDDQ Measurement-Loop Patterns

Table 4: Timings Used for IDD and IDDQ Measurement-Loop Patterns

Parameter	DDR3-1866	DDR3-1600	DDR3-1333	Unit
	13-13-13	11-11-11	9-9-9	
CL	13	11	9	nCK
tCK(min)	1.07	1.25	1.5	ns
nRCD(min)	13	11	9	nCK
nRC(min)	45	39	33	nCK
nRAS(min)	32	28	24	nCK
nRP(min)	13	11	9	nCK
nFAW (1KB)	26	24	20	nCK
nFAW (2KB, 4KB)	33	32	30	nCK
nRRD (1KB)	5	5	4	nCK
nRRD (2KB, 4KB)	6	6	5	nCK
nRFC (1Gb)	103	88	74	nCK
nRFC (2Gb)	150	128	107	nCK
nRFC (4Gb)	243	208	174	nCK

## 1.4.2 Basic IDD and IDDQ Measurement Conditions

Table 5: Basic IDD and IDDQ Measurement Conditions

Parameter	Symbol	Description
Operating one bank active precharge current	IDD0	<p>CKE: H; External clock: on; tCK, nRC, nRAS, CL: see <a href="#">Table 5</a>; BL: 8*<sup>1</sup>; AL: 0; /CS: H between ACT and PRE; Command, address, bank address inputs: partially toggling according to <a href="#">Table 7</a>; Data I/O: MID-LEVEL; DM: stable at 0;</p> <p>Bank activity: cycling with one bank active at a time: 0,0,1,1,2,2,... (see <a href="#">Table 7</a>);</p> <p>Output buffer and RTT: enabled in MR*<sup>2</sup>; ODT signal: stable at 0; Pattern details: see <a href="#">Table 7</a></p>
Operating one bank active-read-precharge current	IDD1	<p>CKE: H; External clock: On; tCK, nRC, nRAS, nRCD, CL: see <a href="#">Table 5</a>; BL: 8*<sup>1,6</sup>; AL: 0; /CS: H between ACT, RD and PRE; Command, address, bank address inputs, data I/O: partially toggling according to <a href="#">Table 8</a>;</p> <p>DM: stable at 0; Bank activity: cycling with one bank active at a time: 0,0,1,1,2,2,... (see <a href="#">Table 8</a>); Output buffer and RTT: enabled in MR*<sup>2</sup>; ODT Signal: stable at 0; Pattern details: see <a href="#">Table 8</a></p>
Precharge standby current	IDD2N	<p>CKE: H; External clock: on; tCK, CL: see <a href="#">Table 5</a>; BL: 8*<sup>1</sup>; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: partially toggling according to <a href="#">Table 9</a>; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in mode registers*<sup>2</sup>; ODT signal: stable at 0; pattern details: see <a href="#">Table 9</a></p>
Precharge standby ODT current	IDD2NT	<p>CKE: H; External clock: on; tCK, CL: see <a href="#">Table 5</a>; BL: 8*<sup>1</sup>; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: partially toggling according to <a href="#">Table 10</a>; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in MR*<sup>2</sup>; ODT signal: toggling according to <a href="#">Table 10</a>; pattern details: see <a href="#">Table 10</a></p>
Precharge standby ODT IDDQ current	IDDQ2NT	Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
Precharge power-down current slow exit	IDD2P0	<p>CKE: L; External clock: on; tCK, CL: see <a href="#">Table 5</a>; BL: 8*<sup>1</sup>; AL: 0; /CS: stable at 1; Command, address, bank address inputs: stable at 0; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: EMR*<sup>2</sup>; ODT signal: stable at 0; precharge power down mode: slow exit*<sup>3</sup></p>
Precharge power-down current fast exit	IDD2P1	<p>CKE: L; External clock: on; tCK, CL: see <a href="#">Table 6</a>; BL: 8*<sup>1</sup>; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: stable at 0; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in MR*<sup>2</sup>; ODT signal: stable at 0; precharge power down mode: fastexit*</p>
Precharge quiet standby current	IDD2Q	<p>CKE: H; External clock: On; tCK, CL: see <a href="#">Table 5</a>; BL: 8*<sup>1</sup>; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: stable at 0; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in MR*<sup>2</sup>; ODT signal: stable at 0</p>
Active standby current	IDD3N	<p>CKE: H; External clock: on; tCK, CL: see <a href="#">Table 5</a>; BL: 8*<sup>1</sup>; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: partially toggling according to <a href="#">Table 9</a>; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks open; output buffer and RTT: enabled in MR*<sup>2</sup>; ODT signal: stable at 0; pattern details: see <a href="#">Table 9</a></p>
Active power-down current	IDD3P	<p>CKE: L; External clock: on; tCK, CL: see <a href="#">Table 5</a>; BL: 8*<sup>1</sup>; AL: 0; /CS: stable at 1; Command, address, bank address inputs: stable at 0; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks open; output buffer and RTT: enabled in MR*<sup>2</sup>; ODT signal: stable at 0</p>
Operating burst read current	IDD4R	<p>CKE: H; External clock: on; tCK, CL: see <a href="#">Table 5</a>; BL: 8*<sup>1,6</sup>; AL: 0; /CS: H between RD; Command, address, bank address Inputs: partially toggling according to <a href="#">Table 11</a>; data I/O: seamless read</p> <p>data burst with different data between one burst and the next one according to <a href="#">Table 11</a>; DM: stable at 0;</p> <p>bank activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see <a href="#">Table 11</a>); Output buffer and RTT: enabled in MR*<sup>2</sup>; ODT signal: stable at 0; pattern details: see <a href="#">Table 11</a></p>
Operating burst read IDDQ current	IDDQ4R	Same definition like for IDD4R, however measuring IDDQ current instead of IDD current

**Table 6: Basic IDD and IDDQ Measurement Conditions (cont'd)**

Parameter	Symbol	Description
Operating burst write current	IDD4W	CKE: H; External clock: on; tCK, CL: see <a href="#">Table 5</a> ; BL: 8* <sup>1</sup> ; AL: 0; /CS: H between WR; command, address, bank address inputs: partially toggling according to <a href="#">Table 12</a> ; data I/O: seamless write data burst with different data between one burst and the next one according to IDD4W Measurement-Loop Pattern table; DM: stable at 0; bank activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see <a href="#">Table 12</a> ); Output buffer and RTT: enabled in MR* <sup>2</sup> ; ODT signal: stable at H; pattern details: see <a href="#">Table 12</a>
Burst refresh current	IDD5B	CKE: H; External clock: on; tCK, CL, nRFC: see <a href="#">Table 5</a> ; BL: 8* <sup>1</sup> ; AL: 0; /CS: H between REF; Command, address, bank address Inputs: partially toggling according to <a href="#">Table 13</a> ; data I/O: MID-LEVEL; DM: stable at 0; bank activity: REF command every nRFC ( <a href="#">Table 13</a> ); output buffer and RTT: enabled in MR* <sup>2</sup> ; ODT signal: stable at 0; pattern details: see <a href="#">Table 13</a>
Self-refresh current: normal temperature range	IDD6	TC: 0 to 85°C; ASR: disabled* <sup>4</sup> ; SRT: Normal* <sup>5</sup> ; CKE: L; External clock: off; CK and /CK: L; CL: see <a href="#">Table 5</a> ; BL: 8* <sup>1</sup> ; AL: 0; /CS, command, address, bank address, data I/O: MID-LEVEL; DM: stable at 0; bank activity: Self-refresh operation; output buffer and RTT: enabled in MR* <sup>2</sup> ; ODT signal: MID-LEVEL
Self-refresh current: extended temperature range	IDD6ET	TC: 0 to 95°C; ASR: Disabled* <sup>4</sup> ; SRT: Extended* <sup>5</sup> ; CKE: L; External clock: off; CK and /CK: L; CL: <a href="#">Table 5</a> ; BL: 8* <sup>1</sup> ; AL: 0; /CS, command, address, bank address, data I/O: MID-LEVEL; DM: stable at 0; bank activity: Extended temperature self-refresh operation; output buffer and RTT: enabled in MR* <sup>2</sup> ; ODT signal: MID-LEVEL
Auto self-refresh current (Optional)	IDD6TC	TC: 0 to 95°C; ASR: Enabled* <sup>4</sup> ; SRT: Normal* <sup>5</sup> ; CKE: L; External clock: off; CK and /CK: L; CL: <a href="#">Table 5</a> ; BL: 8* <sup>1</sup> ; AL: 0; /CS, command, address, bank address, data I/O: MID-LEVEL; DM: stable at 0; bank activity: Auto self-refresh operation; output buffer and RTT: enabled in MR* <sup>2</sup> ; ODT signal: MID-LEVEL
Operating bank interleave read current	IDD7	CKE: H; External clock: on; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see <a href="#">Table 5</a> ; BL: 8* <sup>1,6</sup> ; AL: CL-1; /CS: H between ACT and RDA; Command, address, bank address Inputs: partially toggling according to <a href="#">Table 14</a> ; data I/O: read databursts with different data between one burst and the next one according to <a href="#">Table 14</a> ; DM: stable at 0; bank activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing, see <a href="#">Table 14</a> ; output buffer and RTT: enabled in MR* <sup>2</sup> ; ODT signal: stable at 0; pattern details: see <a href="#">Table 14</a>
RESET low current	IDD8	/RESET: low; External clock: off; CK and /CK: low; CKE: FLOATING; /CS, command, address, bank address, Data IO: FLOATING; ODT signal: FLOATING RESET low current reading is valid once power is stable and /RESET has been low for at least 1ms.

- Notes:
- Burst Length: BL8 fixed by MRS: MR0 bits [1,0] = [0,0].
  - MR: Mode Register  
Output buffer enable: set MR1 bit A12 = 1 and MR1 bits [5, 1] = [0,1];  
RTT\_Nom enable: set MR1 bits [9, 6, 2] = [0, 1, 1]; RTT\_WR enable: set MR2 bits [10, 9] = [1,0].
  - Precharge power down mode: set MR0 bit A12= 0 for Slow Exit or MR0 bit A12 = 1 for fast exit.
  - Auto self-refresh (ASR): set MR2 bit A6 = 0 to disable or 1 to enable feature.
  - Self-refresh temperature range (SRT): set MR0 bit A7= 0 for normal or 1 for extended temperature range.
  - Read burst type: nibble sequential, set MR0 bit A3 = 0

**Table 7: IDD0 Measurement-Loop Pattern**

CK, /CK	CKE	Sub -Loop	Cycle number	Com- Mand	/CS	/RAS	/CAS	/WE	ODT	BA* <sup>3</sup>	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data <sup>2</sup>	
			0	ACT	0	0	1	1	0	0	0	0	0	0	0		
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0		
			3, 4	/D, /D	1	1	1	1	0	0	0	0	0	0	0		
			...	Repeat pattern 1...4 until nRAS - 1, truncate if necessary													
			nRAS	PRE	0	0	1	0	0	0	0	0	0	0	0		
			...	Repeat pattern 1...4 until nRC - 1, truncate if necessary													
			1 X nRC	ACT	0	0	1	1	0	0	0	0	0	F	0		
		0	+0														
			1 X nRC	D, D	1	0	0	0	0	0	0	0	0	F	0		
			+1, 2														
			1 X nRC	/D, /D	1	1	1	1	0	0	0	0	0	F	0		
			+3, 4														
			...	Repeat pattern nRC + 1,...,4 until 1 x nRC + Nras - 1, truncate if necessary													
			1 X nRC	PRE	0	0	1	0	0	0	0	0	0	F	0		
			+ nRAS														
			...	Repeat nRC + 1,...,4 until 2 x nRC - 1, truncate if necessary													
		1	2	nRC Repeat Sub-Loop 0, use BA= 1 instead													
		2	4	nRC Repeat Sub-Loop 0, use BA= 2 instead													
		3	6	nRC Repeat Sub-Loop 0, use BA= 3 instead													
		4	8	nRC Repeat Sub-Loop 0, use BA= 4 instead													
		5	10	nRC Repeat Sub-Loop 0, use BA= 5 instead													
		6	12	nRC Repeat Sub-Loop 0, use BA= 6 instead													
		7	14	nRC Repeat Sub-Loop 0, use BA= 7 instead													

- Notes:
- DM must be driven low all the time. DQS, /DQS are MID-LEVEL.
  - DQ signals are MID-LEVEL.
  - BA: BA0 to BA2.
  - Am: m means Most Significant Bit (MSB) of Row address.

Table 8: IDD1 Measurement-Loop Pattern

CK, /CK	CKE	Sub -Loop	Cycle number	Com- mand	/CS	/RAS	/CAS	/WE	ODT	BA* <sup>3</sup>	A11 -Am	A10	-A7 A9	A3 -A6	A0 -A2	Data* <sup>2</sup>
			0	ACT	0	0	1	1	0	0	0	0	0	0	0	-
			1, 2	D, D	1	0	0	0	0	0	0	0	0	0	0	-
			3, 4	/D, /D	1	1	1	1	0	0	0	0	0	0	0	-
			...	Repeat pattern 1...4 until nRCD - 1, truncate if necessary												
			nRCD	RD	0	1	0	1	0	0	0	0	0	0	0	00000000
			...	Repeat pattern 1..4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	0	0	0	0	0	-
			...	Repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1 x nRC													
		0	+0	ACT	0	0	1	1	0	0	0	0	0	F	0	-
			1 x nRC													
			+ 1, 2	D, D	1	0	0	0	0	0	0	0	0	F	0	-
			1 x nRC													
			+ 3, 4	/D, /D	1	1	1	1	0	0	0	0	0	F	0	-
			...	Repeat pattern nRC + 1,..., 4 until nRC + nRCD - 1, truncate if necessary												
			1 x nRC													
			+ nRCD	RD	0	1	0	1	0	0	0	0	0	F	0	00110011
			...	Repeat pattern nRC + 1,..., 4 until nRC + nRAS - 1, truncate if necessary												
			1 x nRC													
			+ nRAS	PRE	0	0	1	0	0	0	0	0	0	F	0	-
			...	Repeat pattern nRC + 1,..., 4 until 2 x nRC - 1, truncate if necessary												
		1	2	nRC Repeat Sub-Loop 0, use BA= 1 instead												
		2	4	nRC Repeat Sub-Loop 0, use BA= 2 instead												
		3	6	nRC Repeat Sub-Loop 0, use BA= 3 instead												
		4	8	nRC Repeat Sub-Loop 0, use BA= 4 instead												
		5	10	nRC Repeat Sub-Loop 0, use BA= 5 instead												
		6	12	nRC Repeat Sub-Loop 0, use BA= 6 instead												
		7	14	nRC Repeat Sub-Loop 0, use BA= 7 instead												

- Notes:
- DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise MID-LEVEL.
  - Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are MID-LEVEL.
  - BA: BA0 to BA2.
  - Am: m means Most Significant Bit (MSB) of Row address.



**Table 9: IDD2N and IDD3N Measurement-Loop Pattern**

CK, /CK	CKE	Sub -Loop	Cycle number	Com- Mand /CS	/RAS	/CAS	/WE	ODT	BA* <sup>3</sup>	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data* <sup>2</sup>
			0	D 1	0	0	0	0	0	0	0	0	0	0	0
			1	D 1	0	0	0	0	0	0	0	0	0	0	0
			2	/D 1	1	1	1	0	0	0	0	0	F	0	
			3	/D 1	1	1	1	0	0	0	0	0	F	0	
		1	4 to 7	Repeat Sub-Loop 0, use BA= 1 instead											
		2	8 to 11	Repeat Sub-Loop 0, use BA= 2 instead											
		3	12 to 15	Repeat Sub-Loop 0, use BA= 3 instead											
		4	16 to 19	Repeat Sub-Loop 0, use BA= 4 instead											
		5	20 to 23	Repeat Sub-Loop 0, use BA= 5 instead											
		6	24 to 27	Repeat Sub-Loop 0, use BA= 6 instead											
		7	28 to 31	Repeat Sub-Loop 0, use BA= 7 instead											

- Notes:
1. DM must be driven low all the time. DQS, /DQS are MID-LEVEL.
  2. DQ signals are MID-LEVEL.
  3. BA: BA0 to BA2.
  4. Am: m means Most Significant Bit (MSB) of Row address.

**Table 10: IDD2NT and IDDQ2NT Measurement-Loop Pattern**

CK, /CK	CKE	Sub -Loop	Cycle number	Com- Mand /CS	/RAS	/CAS	/WE	ODT	BA* <sup>3</sup>	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data* <sup>2</sup>
			0	D 1	0	0	0	0	0	0	0	0	0	0	0
			1	D 1	0	0	0	0	0	0	0	0	0	0	0
			2	/D 1	1	1	1	0	0	0	0	0	F	0	
			3	/D 1	1	1	1	0	0	0	0	0	F	0	
		1	4 to 7	Repeat Sub-Loop 0, but ODT = 0 and BA= 1											
		2	8 to 11	Repeat Sub-Loop 0, but ODT = 1 and BA= 2											
		3	12 to 15	Repeat Sub-Loop 0, but ODT = 1 and BA= 3											
		4	16 to 19	Repeat Sub-Loop 0, but ODT = 0 and BA= 4											
		5	20 to 23	Repeat Sub-Loop 0, but ODT = 0 and BA= 5											
		6	24 to 27	Repeat Sub-Loop 0, but ODT = 1 and BA= 6											
		7	28 to 31	Repeat Sub-Loop 0, but ODT = 1 and BA= 7											

- Notes:
1. DM must be driven low all the time. DQS, /DQS are MID-LEVEL.
  2. DQ signals are MID-LEVEL.
  3. BA: BA0 to BA2.
  4. Am: m means Most Significant Bit (MSB) of Row address.

**Table 11: IDD4R and IDDQ4R Measurement-Loop Pattern**

CK, /CK	CKE	Sub -Loop	Cycle number	Com- mand	/CS	/RAS	/CAS	/WE	ODT	BA* <sup>3</sup>	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data <sup>2</sup>
			0	RD	0	1	0	1	0	0	0	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
		0	2,3	/D, /D	1	1	1	1	0	0	0	0	0	0	0	-
			4	RD	0	1	0	1	0	0	0	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	0	0	0	F	0	-
			6,7	/D, /D	1	1	1	1	0	0	0	0	0	F	0	-
Toggleing Static H		1	8 to 15	Repeat Sub-Loop 0, but BA= 1												
		2	16 to 23	Repeat Sub-Loop 0, but BA= 2												
		3	24 to 31	Repeat Sub-Loop 0, but BA= 3												
		4	32 to 39	Repeat Sub-Loop 0, but BA= 4												
		5	40 to 47	Repeat Sub-Loop 0, but BA= 5												
		6	48 to 55	Repeat Sub-Loop 0, but BA= 6												
		7	56 to 63	Repeat Sub-Loop 0, but BA= 7												

- Notes:
1. DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise MID-LEVEL.
  2. Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are MID-LEVEL.
  3. BA: BA0 to BA2.
  4. Am: m means Most Significant Bit (MSB) of Row address.

**Table 12: IDD4W Measurement-Loop Pattern**

CK, /CK	CKE	Sub -Loop	Cycle number	Com- Mand	/CS	/RAS	/CAS	/WE	ODT	BA* <sup>3</sup>	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data* <sup>2</sup>
			0	WR	0	1	0	0	1	0	0	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	0	0	0	0	0	-
		0	2,3	/D, /D	1	1	1	1	1	0	0	0	0	0	0	-
			4	WR	0	1	0	0	1	0	0	0	0	F	0	00110011
			5	D	1	0	0	0	1	0	0	0	0	F	0	-
			6,7	/D, /D	1	1	1	1	1	0	0	0	0	F	0	-
Toggleing Static H		1	8 to 15	Repeat Sub-Loop 0, but BA= 1												
		2	16 to 23	Repeat Sub-Loop 0, but BA= 2												
		3	24 to 31	Repeat Sub-Loop 0, but BA= 3												
		4	32 to 39	Repeat Sub-Loop 0, but BA= 4												
		5	40 to 47	Repeat Sub-Loop 0, but BA= 5												
		6	48 to 55	Repeat Sub-Loop 0, but BA= 6												
		7	56 to 63	Repeat Sub-Loop 0, but BA= 7												

- Notes:
1. DM must be driven low all the time. DQS, /DQS are used according to write commands, otherwise MID-LEVEL.
  2. Burst sequence driven on each DQ signal by write command. Outside burst operation, DQ signals are MID-LEVEL.
  3. BA: BA0 to BA2.
  4. Am: m means Most Significant Bit (MSB) of Row address.

**Table 13: IDD5B Measurement-Loop Pattern**

CK, /CK	CKE	Sub -Loop	Cycle number	Com- mand	/CS	/RAS	/CAS	/WE	ODT	BA* <sup>3</sup>	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data* <sup>2</sup>
			0	REF	0	0	0	1	0	0	0	0	0	0	0	-
		0	1, 2	D	1	0	0	0	0	0	0	0	0	0	0	-
			3,4	/D, /D	1	1	1	1	0	0	0	0	0	F	0	-
			5 to 8	Repeat cycles 1...4, but BA= 1												
			9 to 12	Repeat cycles 1...4, but BA= 2												
			13 to 16	Repeat cycles 1...4, but BA= 3												
Toggleing Static H		1	17 to 20	Repeat cycles 1...4, but BA= 4												
			21 to 24	Repeat cycles 1...4, but BA= 5												
			25 to 28	Repeat cycles 1...4, but BA= 6												
			29 to 32	Repeat cycles 1...4, but BA= 7												
		2	33 to nRFC -1	Repeat Sub-Loop 1, until nRFC -1. Truncate, if necessary.												

- Notes:
1. DM must be driven low all the time. DQS, /DQS are MID-LEVEL.
  2. DQ signals are MID-LEVEL.
  3. BA: BA0 to BA2.
  4. Am: m means Most Significant Bit (MSB) of Row address.

Table 14: IDD7 Measurement-Loop Pattern

CK, /CK	CKE	Sub -Loop	Cycle number	Com- mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 -Am	A10	A7 -A9	A3 -A6	A0 -A2	Data* <sup>2</sup>
			0	ACT	0	0	1	1	0	0	0	0	0	0	0	-
			1	RDA	0	1	0	1	0	0	0	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	0	0	0	0	0	-
			...	Repeat above D Command until nRRD -1												
			nRRD	ACT	0	0	1	1	0	1	0	0	0	F	0	-
			nRRD + 1	RDA	0	1	0	1	0	1	0	1	0	F	0	00110011
			nRRD + 2	D	1	0	0	0	0	1	0	0	0	F	0	-
			...	Repeat above D Command until 2 nRRD -1												
		2	2 x nRRD	Repeat Sub-Loop 0, but BA= 2												
		3	3 x nRRD	Repeat Sub-Loop 1, but BA= 3												
		4	4 x nRRD	D	1	0	0	0	0	3	0	0	0	F	0	-
			...	Assert and repeat above D Command until nFAW -1, if necessary												
		5	nFAW	Repeat Sub-Loop 0, but BA= 4												
		6	nFAW + nRRD	Repeat Sub-Loop 1, but BA= 5												
		7	nFAW + 2 x nRRD	Repeat Sub-Loop 0, but BA= 6												
		8	nFAW + 3 x nRRD	Repeat Sub-Loop 1, but BA= 7												
			nFAW	D	1	0	0	0	0	7	0	0	0	F	0	-
		9	+ 4 x nRRD	Assert and repeat above D Command until 2 x nFAW -1, if necessary												
			2 x nFAW +0	ACT	0	0	1	1	0	0	0	0	0	F	0	-
			2 x nFAW +1	RDA	0	1	0	1	0	0	0	1	0	F	0	00110011
			2 x nFAW D +2	D	1	0	0	0	0	0	0	0	0	F	0	-
			...	Repeat above D Command until 2 x nFAW + nRRD -1												
			2 x nFAW + nRRD	ACT	0	0	1	1	0	1	0	0	0	0	0	-
			2 x nFAW + nRRD + 1	RDA	0	1	0	1	0	1	0	1	0	0	0	00000000
			2 x nFAW D + nRRD + 2	D	1	0	0	0	0	1	0	0	0	0	0	-
			...	Repeat above D Command until 2 x nFAW + 2 x nRRD -1												
		12	2 x nFAW +2 x nRRD	Repeat Sub-Loop 10, but BA= 2												
		13	2 x nFAW + 3 x nRRD	Repeat Sub-Loop 11, but BA= 3												
		14	2 x nFAW D + 4 x nRRD	D	1	0	0	0	0	3	0	0	0	0	0	-
			...	Assert and repeat above D Command until 3 x nFAW -1, if necessary												
		15	3 x nFAW	Repeat Sub-Loop 10, but BA= 4												
		16	3 x nFAW +nRRD	Repeat Sub-Loop 11, but BA= 5												
		17	3 x nFAW + 2 x nRRD	Repeat Sub-Loop 10, but BA= 6												
		18	3 x nFAW + 3 x nRRD	Repeat Sub-Loop 11, but BA= 7												
			3 x nFAW D	D	1	0	0	0	0	7	0	0	0	0	0	-
		19	+ 4 x nRRD	Assert and repeat above D Command until 4 x nFAW -1, if necessary												

- Notes:
- DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise MID-LEVEL.
  - Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are MID-LEVEL.
  - BA: BA0 to BA2.
  - Am: m means Most Significant Bit (MSB) of Row address.

## 2 Electrical Specifications(x4/x8/x16)

### 2.1 DC Characteristics

Table 15: DC Characteristics 1 (TC = 0°C to +85°C)

Parameter	Symbol	Data rate (Mbps)	x 4	x8	x16	Unit	Notes
			max.	max.	max.		
Operating current (ACT-PRERE)	IDD0	1866	70	70	80	mA	
		1600	65	65	75		
		1333	60	60	70		
Operating current (ACT-READ-PRE)	IDD1	1866	85	85	100	mA	
		1600	80	80	95		
		1333	75	75	90		
Precharge power-down standby current	IDD2P1	1866	35	35	35	mA	Fast PD Exit
		1600	35	35	35		
		1333	35	35	35		
	IDD2P0	1866	20	20	20	mA	Slow PD Exit
		1600	20	20	20		
		1333	20	20	20		
Precharge standby current	IDD2N	1866	45	45	45	mA	
		1600	45	45	45		
		1333	45	45	45		
Precharge standby ODT current	IDD2NT	1866	45	45	45	mA	
		1600	45	45	45		
		1333	45	45	45		
Precharge quiet standby current	IDD2Q	1866	45	45	45	mA	
		1600	45	45	45		
		1333	45	45	45		
Active power-down current (Always fast exit)	IDD3P	1866	40	40	40	mA	
		1600	39	39	39		
		1333	37	37	37		
Active standby current	IDD3N	1866	55	55	55	mA	
		1600	55	55	55		
		1333	55	55	55		
Operating current (burst read operating)	IDD4R	1866	140	145	180	mA	
		1600	120	125	160		
		1333	105	110	145		
Operating current (Burst write operating)	IDD4W	1866	145	150	205	mA	
		1600	125	130	185		
		1333	110	115	170		
Burst refresh current	IDD5B	1866	260	260	260	mA	
		1600	250	250	250		
		1333	250	250	250		
All bank interleave read current	IDD7	1866	210	220	260	mA	
		1600	200	210	250		
		1333	190	200	230		
RESET low current	IDD8	1866/1600/1333	17	17	17	mA	

### Self-Refresh Current (TC = 0°C to +85°C)

Parameter	Symbol	Grade	x 4	x8	x16	Unit	Notes
			max.	max.	max.		
Self-refresh current normal temperature range	IDD6	1866/1600/1333	22	22	22	mA	
Self-refresh current extended temperature range	IDD6E	1866/1600/1333	25	25	25	mA	
Auto self-refresh current (Optional)	IDD6TC	1866/1600/1333	—	—	—	mA	

## 2.2 Pin Capacitance

Table 16: Pin Capacitance [DDR3-1333 to 1600] (TC = 25°C)

Parameter	Symbol	DDR3-1866		DDR3L-1600		DDR3L-1333		Units	Notes
		Min	Max	Min	Max	Min	Max		
Input/output capacitance	CIO	1.4	2.2	1.4	2.2	1.4	2.3	pF	1, 2
Input capacitance, CK and /CK	CCK	0.8	1.4	0.8	1.4	0.8	1.4	pF	2
Input capacitance delta, CK and /CK	CDCK	0	0.15	0	0.15	0	0.15	pF	2, 3
Input/output capacitance delta, DQS and /DQS	CDDQS	0	0.15	0	0.15	0	0.15	pF	2, 4
Input capacitance, (control, address, command, input-only pins)	CI	0.75	1.2	0.75	1.2	0.75	1.3	pF	2, 5
Input capacitance delta, (All control input-only pins)	CDI_CTRL_	-0.4	0.2	-0.4	0.2	-0.4	0.2	pF	2, 6, 7
Input capacitance delta, (All address/command input-only pins)	CDI_ADD_CMD	-0.4	0.4	-0.4	0.4	-0.4	0.4	pF	2, 8, 9
Input/output capacitance delta, DQ,DM, DQS, /DQS, TDQS, /TDQS	CDIO	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2, 10
Input/output capacitance of ZQ pin	CZQ	–	3	–	3	–	3	pF	2, 11

Notes: 1. Although the DM, TDQS and /TDQS pins have different functions, the loading matches DQ and DQS.

2. VDD, VDDQ, VSS, VSSQ applied and all other pins floating (except the pin under test, CKE, /RESET and ODT as necessary). VDD = VDDQ = 1.35V, VBIAS=VDD/2 and ondie termination off.
3. Absolute value of CCK-C/CK.
4. Absolute value of CIO(DQS)-CIO(/DQS).
5. CI applies to ODT, /CS, CKE, A0-A15, BA0-BA2, /RAS, /CAS and /WE.
6. CDI\_CTRL applies to ODT, /CS and CKE.
7.  $CDI\_CTRL = CI(CTRL) - 0.5 \times (CI(CK) + CI(/CK))$ .
8. CDI\_ADD\_CMD applies to A0-A15, BA0-BA2, /RAS, /CAS and /WE.
9.  $CDI\_ADD\_CMD = CI(ADD\_CMD) - 0.5 \times (CI(CK) + CI(/CK))$ .
10.  $CDIO = CIO(DQ,DM) - 0.5 \times (CIO(DQS) + CIO(/DQS))$ .
11. Maximum external load capacitance on ZQ pin: 5pF.

### 2.3 Standard Speed Bins

Table 17: DDR3-1866 Speed Bins

Speed Bin		DDR3-1866		Unit	Notes
CL-tRCD-tRP		13-13-13			
Symbol	/CAS write latency	min	max		
tAA		13.91	20	ns	
tRCD		13.91	–	ns	
tRP		13.91	–	ns	
tRC		47.91	–	ns	
tRAS		34.0	9 x tREFI	ns	8
tCK(avg) @CL=5	CWL = 5	3.0	3.3	ns	1, 2, 3, 8
	CWL = 6, 7, 8,9	Reserved	Reserved	ns	4
tCK(avg) @CL=6	CWL = 5	2.5	3.3	ns	1, 2, 3, 8
	CWL = 6	Reserved	Reserved	ns	4
	CWL = 7, 8,9	Reserved	Reserved	ns	4
tCK(avg) @CL=7	CWL = 5	Reserved	Reserved	ns	4
	CWL = 6	1.875	2.5	ns	1, 2, 3, 8
	CWL = 7,8,9	Reserved	Reserved	ns	4
tCK(avg) @CL=8	CWL = 5	Reserved	Reserved	ns	4
	CWL = 6	1.875	2.5	ns	1, 2, 3, 8
	CWL = 7	Reserved	Reserved	ns	4
	CWL = 8,9	Reserved	Reserved	ns	4
tCK(avg) @CL=9	CWL = 5, 6	Reserved	Reserved	ns	4
	CWL= 7	1.5	1.875	ns	1, 2, 3, 8
	CWL= 8	Reserved	Reserved	ns	4
	CWL= 9	Reserved	Reserved	ns	4
tCK(avg) @CL=10	CWL = 5, 6	Reserved	Reserved	ns	4
	CWL= 7	1.5	1.875	ns	1,2,3,8
	CWL= 8	Reserved	Reserved	ns	4
tCK(avg) @CL=11	CWL = 5, 6, 7	Reserved	Reserved	ns	4
	CWL= 8	1.25	1.5	ns	1, 2, 3, 8
	CWL= 9	Reserved	Reserved	ns	4
tCK(avg) @CL=12	CWL = 5, 6, 7,8	Reserved	Reserved	ns	4
	CWL= 9	Reserved	Reserved	ns	4
tCK(avg) @CL=13	CWL = 5, 6, 7,8	Reserved	Reserved	ns	4
	CWL= 9	1.07	1.25	ns	4
Supported CL settings			5, 6, 7, 8, 9, 10, 11,13	nCK	1,2,3,8
Supported CWL settings			5, 6, 7, 8,9	nCK	

Table 18: DDR3-1600 Speed Bins

Speed Bin		DDR3-1600			
CL-tRCD-tRP		11-11-11			
Symbol	/CAS write latency	min	max	Unit	Notes
tAA		13.75 (13.125)	20	ns	9
tRCD		13.75 (13.125)	–	ns	9
tRP		13.75 (13.125)	–	ns	9
tRC		48.75 (48.125)	–	ns	9
tRAS		35	9 × tREFI	ns	8
tCK(avg) @CL=5	CWL = 5	3.0	3.3	ns	1, 2, 3, 4, 7, 10
	CWL = 6, 7, 8	Reserved	Reserved	ns	4
tCK(avg) @CL=6	CWL = 5	2.5	3.3	ns	1, 2, 3, 7
	CWL = 6	Reserved	Reserved	ns	4
	CWL = 7, 8	Reserved	Reserved	ns	4
tCK(avg) @CL=7	CWL = 5	Reserved	Reserved	ns	4
	CWL = 6	1.875	< 2.5	ns	1, 2, 3, 4, 7
	CWL = 7	Reserved	Reserved	ns	4
	CWL = 8	Reserved	Reserved	ns	4
tCK(avg) @CL=8	CWL = 5	Reserved	Reserved	ns	4
	CWL = 6	1.875	< 2.5	ns	1, 2, 3, 7
	CWL = 7	Reserved	Reserved	ns	4
	CWL = 8	Reserved	Reserved	ns	4
tCK(avg) @CL=9	CWL = 5, 6	Reserved	Reserved	ns	4
	CWL = 7	1.5	< 1.875	ns	1, 2, 3, 4, 7
	CWL = 8	Reserved	Reserved	ns	4
tCK(avg) @CL=10	CWL = 5, 6	Reserved	Reserved	ns	4
	CWL = 7	1.5	< 1.875	ns	1, 2, 3, 7
	CWL = 8	Reserved	Reserved	ns	4
tCK(avg) @CL=11	CWL = 5, 6, 7	Reserved	Reserved	ns	4
	CWL = 8	1.25	< 1.5	ns	1,2,3
Supported CL settings		5, 6, 7, 8, 9, 10, 11		nCK	
Supported CWL settings		5, 6, 7, 8		nCK	



Table 19 DDR3-1333 Speed Bins

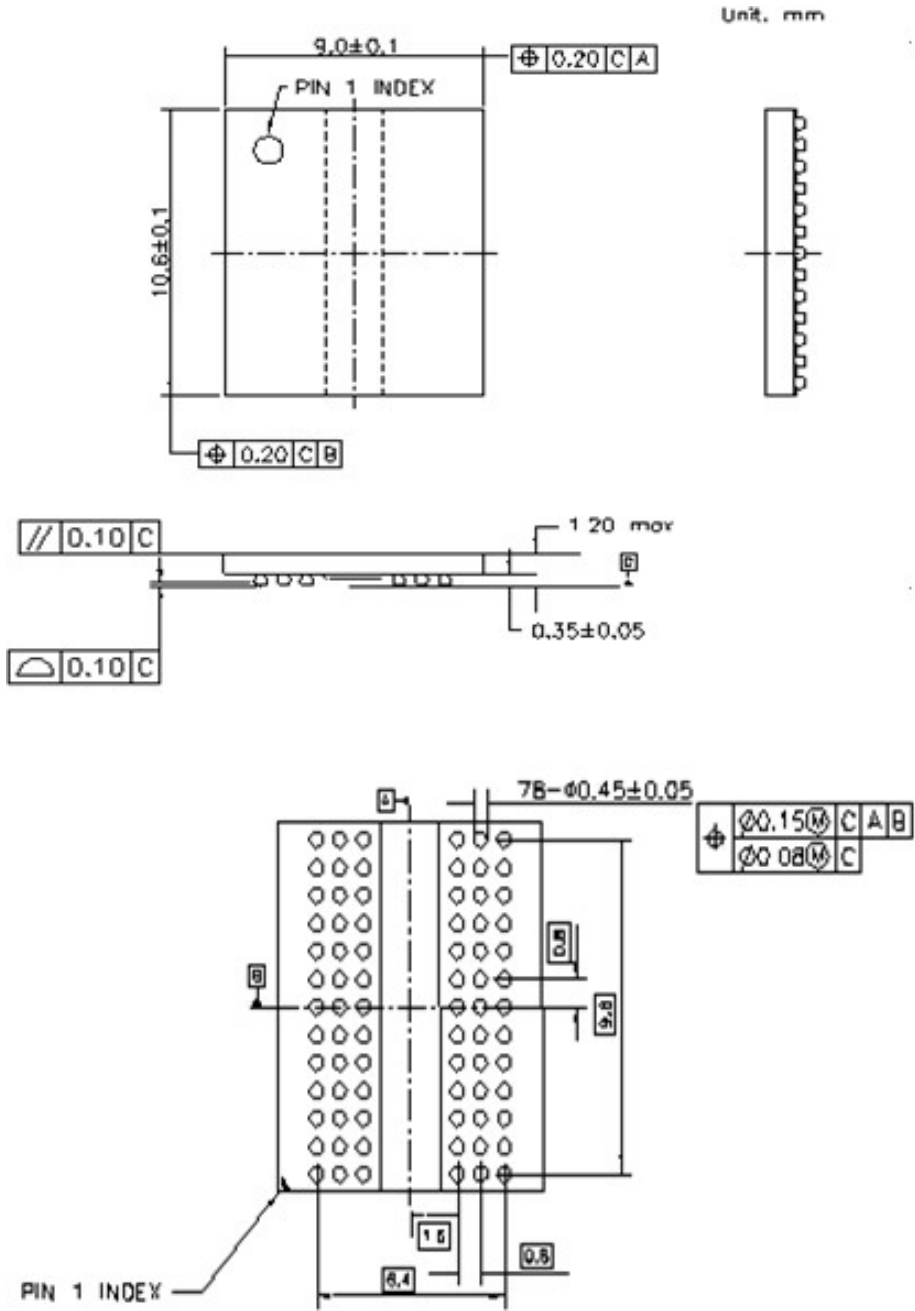
Speed Bin		DDR3-1333			
CL-tRCD-tRP		9-9-9			
Symbol	/CAS write latency	min	max	Unit	Notes
tAA		13.5 (13.125)	20	ns	9
tRCD		13.5 (13.125)	–	ns	9
tRP		13.5 (13.125)	–	ns	9
tRC		49.5 (49.125)	–	ns	9
tRAS		36	9 x tREFI	ns	8
tCK(avg) @CL=5	CWL = 5	3.0	3.3	ns	1, 2, 3, 4, 6, 10
	CWL = 6, 7	Reserved	Reserved	ns	4
tCK(avg) @CL=6	CWL = 5	2.5	3.3	ns	1, 2, 3, 6
	CWL = 6	Reserved	Reserved	ns	4
	CWL = 7	Reserved	Reserved	ns	4
tCK(avg) @CL=7	CWL = 5	Reserved	Reserved	ns	4
	CWL = 6	1.875	< 2.5	ns	1, 2, 3, 4, 6
	CWL = 7	Reserved	Reserved	ns	4
tCK(avg) @CL=8	CWL = 5	Reserved	Reserved	ns	4
	CWL = 6	1.875	< 2.5	ns	1, 2, 3, 6
	CWL = 7	Reserved	Reserved	ns	4
tCK(avg) @CL=9	CWL = 5, 6	Reserved	Reserved	ns	4
	CWL = 7	1.5	< 1.875	ns	1, 2, 3, 4
tCK(avg) @CL=10	CWL = 5, 6	Reserved	Reserved	ns	4
	CWL = 7	1.5	< 1.875	ns	1, 2, 3
Supported CL settings		5, 6, 7, 8, 9, 10		nCK	
Supported CWL settings		5, 6, 7		nCK	

- Notes: 1. The CL setting and CWL setting result in  $t_{CK(ave)}^{min}$  and  $t_{CK(ave)}^{max}$  requirements. When making a selection of  $t_{CK(ave)}$ , both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2.  $t_{CK(ave)}^{min}$  limits: Since /CAS latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard  $t_{CK(ave)}$  value (3.0, 2.5, 1.875, 1.5, or 1.25ns) when calculating  $CL(nCK) = t_{AA}(ns) / t_{CK(ave)}(ns)$ , rounding up to the next 'Supported CL'.
3.  $t_{CK(ave)}^{max}$  limits: Calculate  $t_{CK(ave)} + t_{AA}(max)/CL$  selected and round the resulting  $t_{CK(ave)}$  down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875ns or 1.25ns). This result is  $t_{CK(ave)}^{max}$  corresponding to CL selected.
4. Reserved' settings are not allowed. User must program a different value.
5. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table DDR3-1333 Speed Bins which is not subject to production tests but verified by design/characterization.
6. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table DDR3-1600 Speed Bins which is not subject to production tests but verified by design/characterization.
7.  $t_{REFI}$  depends on operating case temperature (TC).
8. For devices supporting optional down binning to CL = 7 and CL = 9,  $t_{AA}/t_{RCD}/t_{RP}(min)$  must be 13.125 ns or lower. SPD settings must be programmed to match.
9. DDR3-800 AC timing apply if DRAM operates at lower than 800 MT/s data rate.

3. Package Drawing

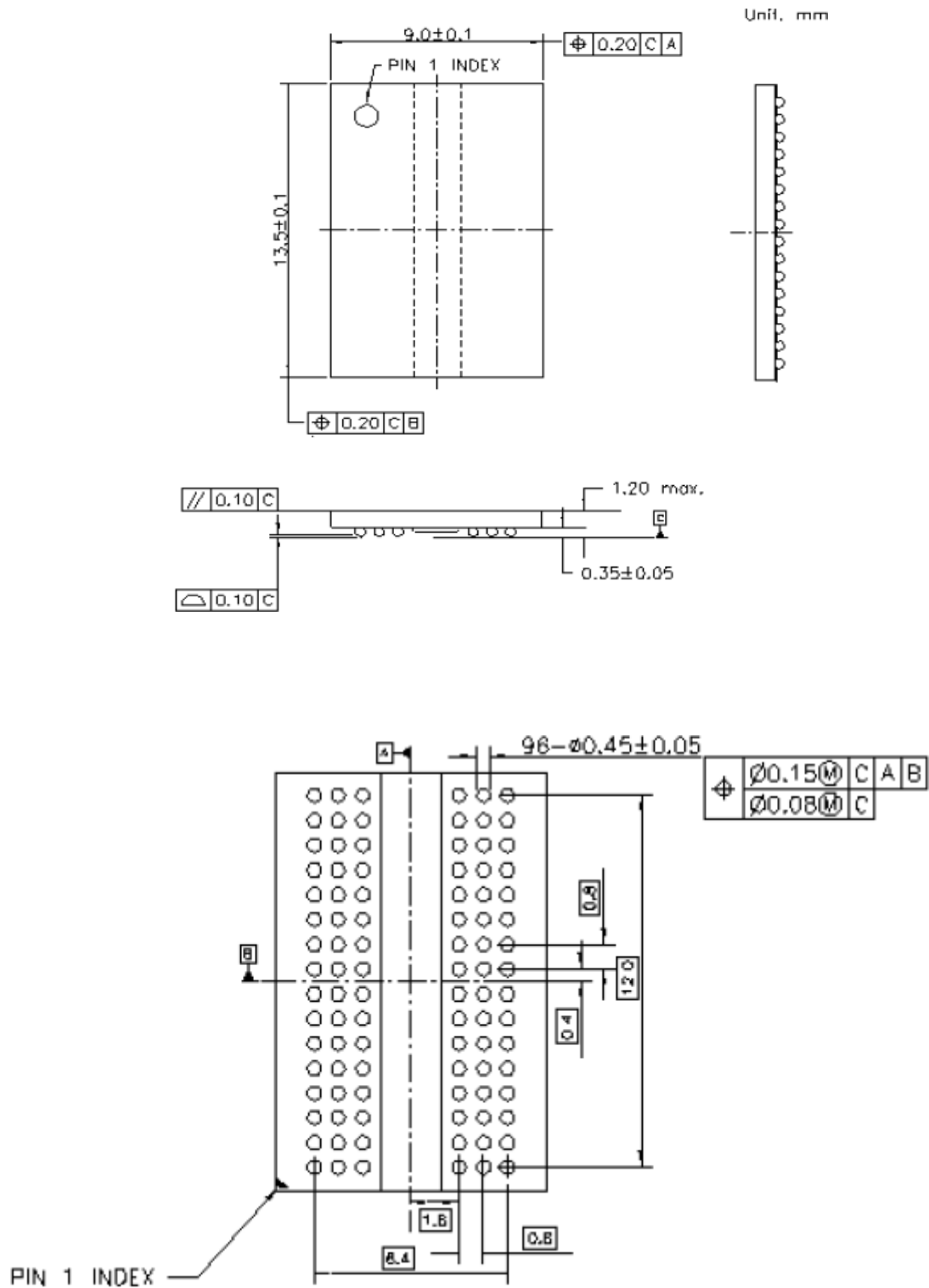
3.1 78-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu)



3.2 96-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu)



#### 4. Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the 4G bits DDR3 SDRAM.

## NOTES FOR CMOS DEVICES



## PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.



## HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.



## STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.